IN THE CLAIMS

Please cancel Claims 1-17, 31-40, and 44-46 without prejudice, amend Claims 41 and 43, and add new Claims 47-68 as follows:

1.- 40. (Cancelled)

41. (Currently amended) A user-configurable processing device having a user-configured processor interface device and digital signal processing (DSP) core associated therewith, comprising:

a reduced instruction set computer (RISC) core in operative communication with said interface device;

at least one memory port, said at least one memory port adapted to transfer data and signals to and from a storage device;

at least one function port, said at least one function port adapted to transfer data and signals to and from a macro function;

a data transfer fabric adapted to transfer data and signals between said at least one memory port and said at least one function port, and

an arbitration unit adapted to arbitrate access to various portions of said storage device by said macro function;

wherein said DSP core is specifically configured by said user to inter-operate with at least one of (i) an ~~the~~ instruction and operand decode mechanism, (ii) an auxiliary register, and (iii) on-core memory resources ~~of~~ associated with said RISC processor.

42. (Previously presented) A processor device having a processor interface device associated therewith, comprising:

a processor core in operative communication with said interface device;

at least one memory port, said at least one memory port adapted to transfer data and signals to and from a storage device;

at least one function port, said at least one function port adapted to transfer data and signals to and from a macro function;

at least one function controller operatively coupled to said at least one function port, said controller being adapted to control at least one aspect of the operation of said at least one port;

a data transfer fabric adapted to transfer data and signals between said at least one memory port and said at least one function port,

an arbitration unit adapted to arbitrate access to various portions of said storage device by said macro function;

wherein said processor core comprises a configuration determined at least in part based on user selections, said selections causing a prototype core description to be modified in order to produce said configuration.

43. (Currently amended) A user-configurable processing device having a first processor core, a user-configured processor interface device, and second core associated therewith, the interface comprising:

at least one memory port, said at least one memory port adapted to transfer data and signals to and from a storage device;

at least one function port and associated function controller, said at least one function port and controller cooperating to transfer data and signals to and from a macro function;

a data transfer medium adapted to transfer data and signals between said at least one memory port and said at least one function port, and

an arbitration unit adapted to arbitrate access to various portions of said storage device by said macro function;

wherein said second processor core is specifically configured by said user at time of design to inter-operate with <u>an</u> ~~the~~ instruction and operand decode mechanism, auxiliary register, and on-core memory resources of said first processor core.

44. – 46. (Cancelled)

47. (New) The processing device of Claim 41, wherein said configuring of said DSP core by said user is performed substantially at the time of design of said processing device.

48. (New) The processing device of Claim 41, wherein said DSP core is substantially deterministic in its operation.

49. (New) The processing device of Claim 41, wherein said macro function comprises said DSP core.

50. (New) The processing device of Claim 41, wherein said DSP core is adapted to perform operations in support of third-generation (3G) communications algorithms.

51. (New) The processing device of Claim 41, wherein said processing device comprises a System-on-Chip (SoC) integrated circuit device comprising a single die.

52. (New) The processing device of Claim 41, wherein said RISC core comprises a user-extendable core.

53. (New) The processing device of Claim 41, wherein said RISC core is designed by at least generating a customized description language model by the method comprising:

receiving one or more inputs from a user for at least one customized parameter of the RISC core;

providing at least one prototype description of the RISC core for which a model is being generated; and

generating through an automated process a customized description language model based on the least one customized parameter and the at least one prototype description, said act of generating comprising modifying at least portions of said at least one prototype description.

54. (New) The processor device of Claim 42, wherein said processor core comprises a user-extended RISC processor core.

55. (New) The processor device of Claim 42, wherein said processor core is adapted to perform operations in support of third-generation (3G) communications algorithms.

56. (New) The processor device of Claim 42, wherein said macro function is adapted to perform operations in support of third-generation (3G) communications algorithms.

57. (New) The processor device of Claim 42, wherein said processor device comprises a System-on-Chip (SoC) integrated circuit device comprising a single die.

58. (New) The processor device of Claim 42, wherein said modification of said prototype description comprises adding extension logic and at least one extension instruction.

59. (New) The processor device of Claim 42, wherein said macro function comprises a digital signal processing (DSP) application.

60. (New) The processing device of Claim 43, wherein said data transfer medium comprises a cross-bar switch.

61. (New) The processing device of Claim 43, wherein said processing device comprises a System-on-Chip (SoC) integrated circuit device comprising a single die.

62. (New) The processing device of Claim 61, wherein said macro function comprises a macro block of said integrated circuit device.

63. (New) The processing device of Claim 43, wherein said macro function comprises a soft function being at least party configurable by a user.

64. (New) The processing device of Claim 43, wherein said macro function comprises a software-based function running on one of said first or second processor cores.

65. (New) The processing device of Claim 64, wherein said software-based function is selected from the group consisting of: (i) convolutional encoding or decoding; (ii) Viterbi coding or decoding; and (iii) Turbo coding or decoding.

66. (New) A user-configurable processing means having a user-configured processor interface means and digital signal processing (DSP) core associated therewith, comprising:

reduced instruction set computer (RISC) core means in operative communication with said interface means;

at least one first means for transferring data and signals to and from a storage device;

at least one second means for transferring data and signals to and from a macro function;

means for transferring data and signals between said at least one first means and said at least one second means; and

an arbitration means adapted to arbitrate access to various portions of said storage device by said macro function;

wherein said DSP core is specifically configured by said user to interoperate with at least one of (i) an instruction and operand decode means, (ii) auxiliary register means, and (iii) on-core memory means of said RISC means.

67. (New) A processing device having a processor interface device associated therewith, comprising:

a processor core in operative communication with said interface device;

at least one memory port, said at least one memory port adapted to transfer data and signals to and from a storage device;

at least one function port, said at least one function port adapted to transfer data and signals to and from a macro function;

at least one function controller operatively coupled to said at least one function port, said controller being adapted to control at least one aspect of the operation of said at least one port;

data transfer means adapted to transfer data and signals between said at least one memory port and said at least one function port,

arbitration means adapted to arbitrate access to various portions of said storage device by said macro function;

wherein said processor core comprises a configuration determined at least in part based on user selections, said selections causing a prototype core description to be modified in order to produce said configuration.

68. (New) A user-configurable processing means having a first processor core, a user-configured processor interface means, and second core associated therewith, the interface means comprising:

at least one memory port means, said at least one memory port means adapted for the transfer of data and signals to and from a storage device;

at least one function port means and associated controller means, said at least one function port means and controller means cooperating to transfer data and signals to and from a macro function;

data transfer means adapted to transfer data and signals between said at least one memory port means and said at least one function port means, and

arbitration means adapted to arbitrate access to various portions of said storage device by said macro function;

wherein said second processor core is specifically configured by said user at time of design to inter-operate with an instruction and operand decode mechanism, auxiliary register, and on-core memory resources of said first processor core.